SN74LS07N

Product Introduction

The SN74LS07N is an integrated circuit that integrates six sets of TTL buffers. Each buffer is independent of each other, and the output port of the buffer is an open drain output structure. The minimum withstand voltage of the high-voltage collector is up to 25V. It can be used as an input interface for driving high-voltage circuits (such as driving MOS) or for driving high-current loads (such as lamps, motors or relays).

Product Features

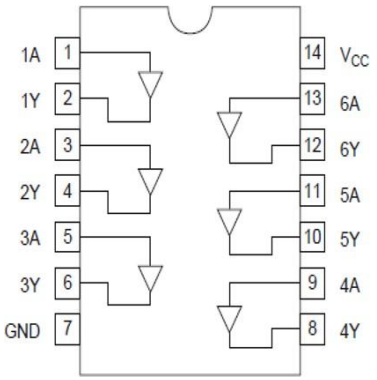
- The minimum withstand voltage of High Voltage Collector open drain output is 25V
- Greater driving powe
- Input clamping diode to simplify system design
- Fully compatible with TTL/DTL input and output logic level
- Package : DIP14, SOP14

Product Applications

- Digital logic driver
- Industrial control applications
- Other application areasBattery-powered equipment

Package and Pin Assignment

SOP14 or DIP14.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input A1	14	Supply VCC
2	Output Y1	13	Input A6
3	Input A2	12	Output Y6
4	Output Y2	11	Input A5
5	Input A3	10	Output Y5
6	Output Y3	9	Input A4
7	Supply GND	8	Output Y4

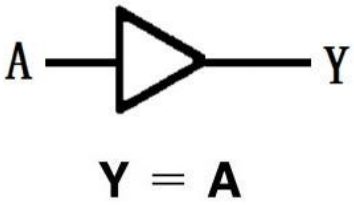


Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	5.5	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
welding temperature	T_W	260	℃,10s

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Block Diagram



Y = A

Function Table

Input	Output
A	Y
L	L
H	H

H = High Logic Level

L = Low Logic Level

Recommended Operating Conditions

Item	Symbol	Min	Tpy	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IH}	2	—	—	V
	V_{IL}	—	—	0.7	V
Output voltage	V_{OH}	—	—	25	V
Output current	I_{OL}	—	—	48	mA
Operating temperature	T_a	0	—	60	℃

Electrical Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Leakage current	I_{OH}	—	—	250	uA	VCC=4.75V, V_{IH}=2V, V_{OH}=25V	
Output voltage	V_{OL}	—	0.15	0.4	V	I_{OL}=24mA	VCC=4.75V, V_{IL}=0.7V
		—	0.20	0.5		I_{OL}=48mA	
Input current	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	I_{IL}	—	-0.20	-0.4	mA	VCC=5.25V, V_I=0.4V	
Supply current	I_{CCH}	—	—	41	mA	VCC=5.25V, all V_I=VCC	
	I_{CCL}	—	—	30	mA	VCC=5.25V, all V_I=GND	
Input clamp voltage	V_{IK}	—	0.9	-1.5	V	VCC=4.75V, I_I=-18mA	

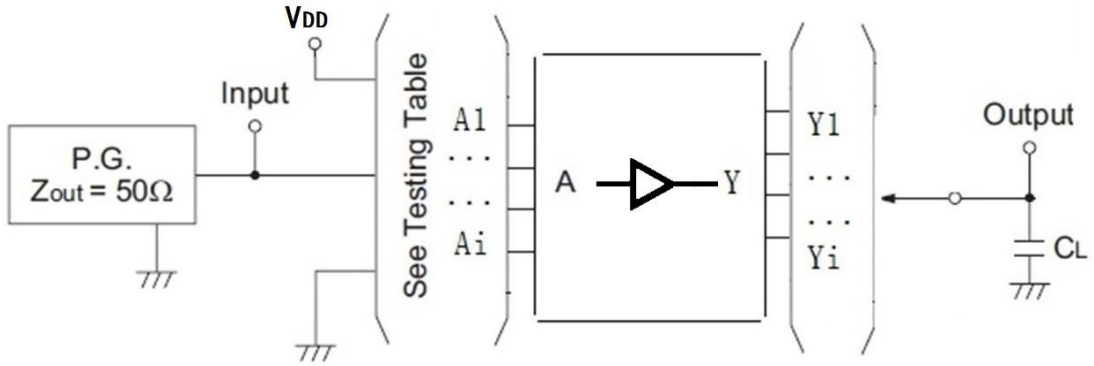
Switching Characteristics

(T_A=25℃, Unless specified)

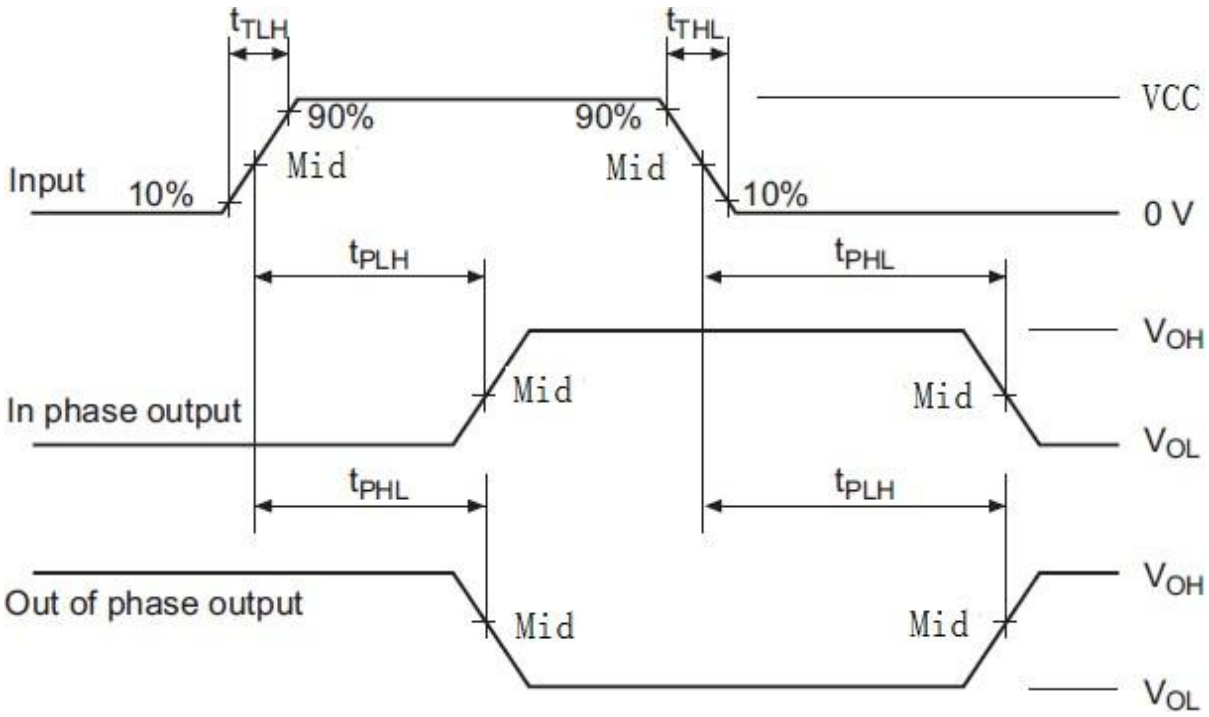
Item	Symbol	Min	Tpy	Max	Unit	Conditions
Propagation delay time	t_{PLH}	—	70	—	ns	VCC=5V, CL=16pF, RL=2KΩ
	t_{PHL}	—	10	—	ns	

■ Testing Method

1、Test Circuit



2、Waveform



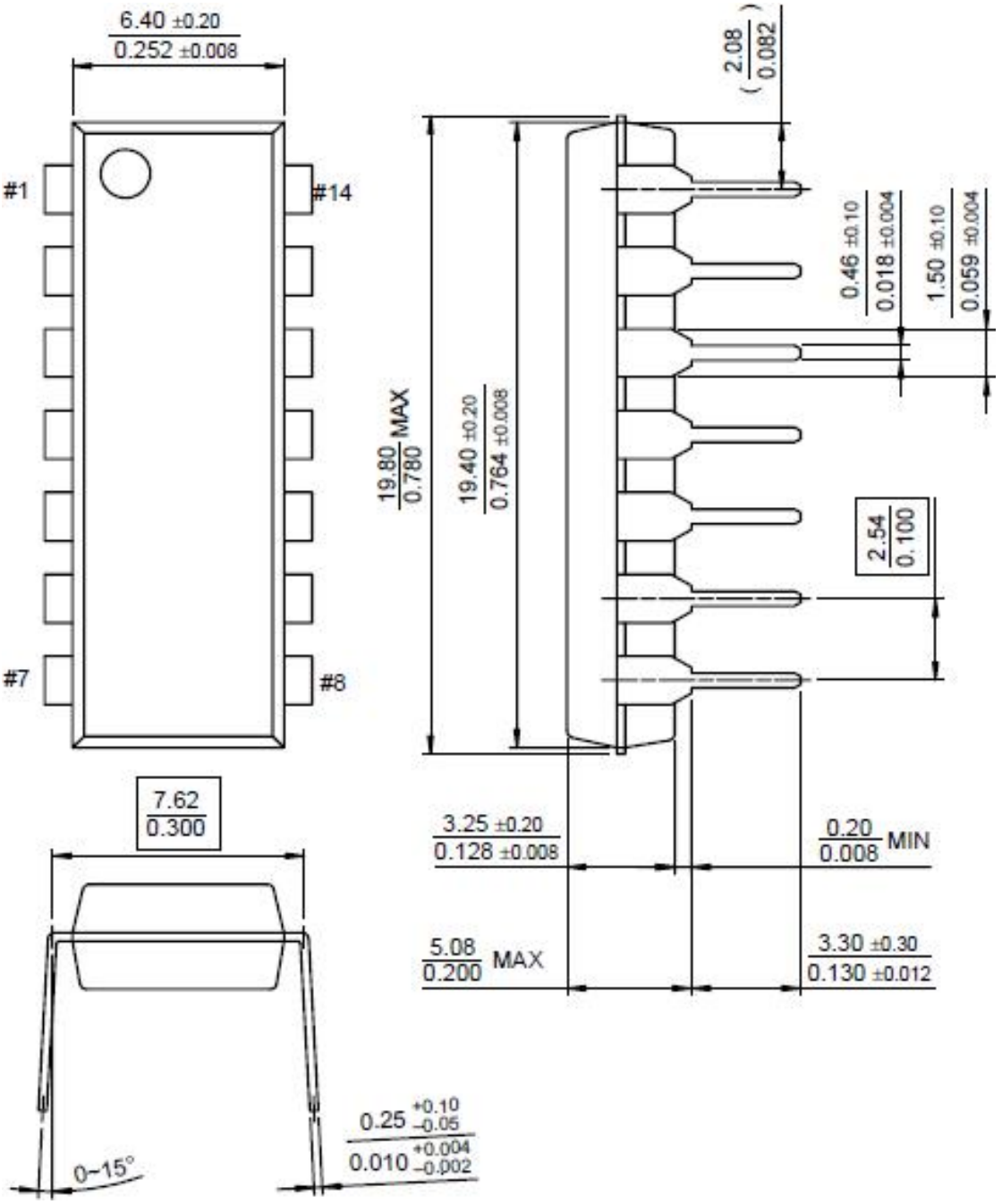
Note:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. Input: port input level, f=500kHz, D=50%, tTLH=tTHL or less 20ns;
4. Output: Y output test port (Out of Phase Output, In Phase Output)

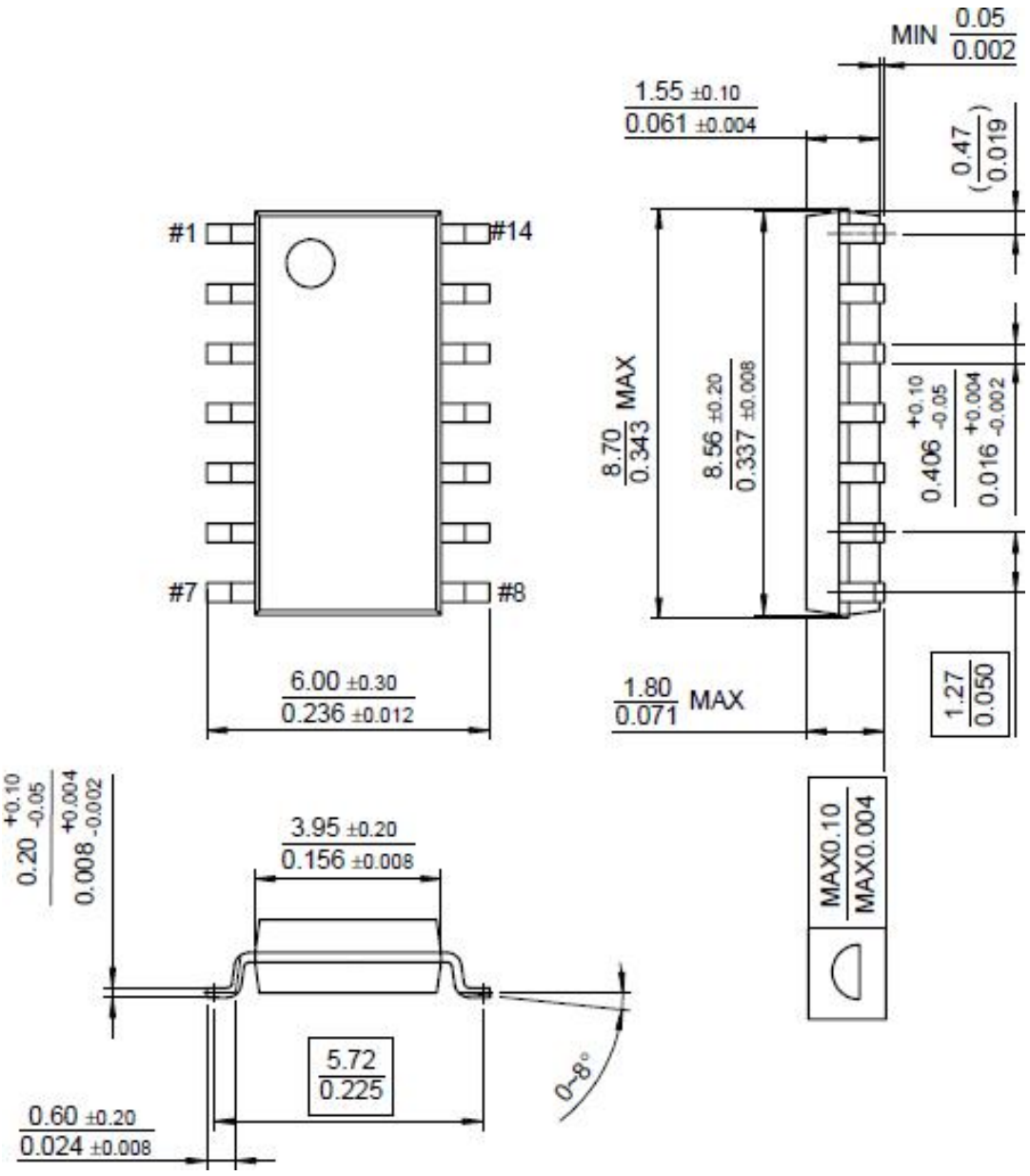
■ Package Dimensions

Unit：mm /inch

DIP14



SOP14


MIN 0.05 0.002
1.55 ±0.10
0.061 ±0.004
0.47 (0.019)
#1
#14
#7
#8
8.70 MAX 0.343
8.56 ±0.20
0.337 ±0.008
0.406 +0.10 -0.05
0.016 +0.004 -0.002
6.00 ±0.30
0.236 ±0.012
1.80 MAX
0.071
1.27
0.050
0.20 +0.10 -0.05
0.008 +0.004 -0.002
3.95 ±0.20
0.156 ±0.008
MAX0.10
MAX0.004
5.72
0.225
0~8°
0.60 ±0.20
0.024 ±0.008